REMARKS

In response to the pending Office Action, claims 1-5, 9, 10, and 15 are amended. Claims 1-16 are now active in this application. No new matter has been added. Claims 1 and 15 are independent claims. The amendments are supported by, at a minimum, FIG. 4.

Claims 9, 15, and 16 were objected to for informalities. Applicants submit that this objection has been overcome by the foregoing amendments.

Claim 1 was rejected under 35 U.S.C. § 112, second paragraph, as allegedly indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Applicants respectfully traverse.

Specifically, the Office Action, at page 3 asserts that, "[a] broad range or limitation together with a narrow range or limitation that falls within the broad range or limitation is considered indefinite." However, Applicants submit that claim 1 has been amended to clarify that, "a conductor exhibits an electron concentration negatively correlated with temperature in **a temperature range which has a width of 100°C or more** and is included within **a temperature region from 0°C to 300°C**."

As an illustrative and non-limiting example of claim 1, a temperature range from 50°C to 160°C has a "width" of 110°C (160°C – 50°C), and satisfies the claim 1 requirement that "a temperature range which has a width of 100°C or more,"

Additionally, this temperature range from 50°C to 160°C has a low endpoint (50°C) which is greater than or equal to 0°C (the low endpoint of the temperature region), and has a high endpoint (160°C) which is lower than or equal to 300°C (the high endpoint of the temperature region), and satisfies the claim 1 requirement that the temperature range "is included within a temperature region from 0°C to 300°C."

Other illustrative examples of claim 1 comprise temperature ranges from: 0°C to 150°C; or 75°C to 250°C; or 99°C to 300°C.

Thus, Applicants submit that claim 1 is definite, and this rejection should be withdrawn.

Claims 1-6, 8, and 13 were rejected under 35 U.S.C. § 102(b) as allegedly anticipated by Ando et al. (JP 2001-007385), **or in the alternative, under 35 U.S.C. § 103(a)** as allegedly obvious over Ando et al. (JP 2001-007385) apparently in view of alleged inherency. Applicants respectfully traverse the rejection, and traverse the alleged inherency. Note that the Examiner has provided an English version of Ando which has been machine translated.

Claim 7 was rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Ando in view of Hasegawa et al. (U.S. Patent App. Publication 2002/0127405). Applicants respectfully traverse.

Claims 9, 11, 14, and 15 were rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Ando in view of Yoshida (U.S. Patent 6,340,393). Applicants respectfully traverse.

Claims 10 and 16 were rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Ando in view of Yoshida and further in view of Yasegawa. Applicants respectfully traverse.

Claim 12 was rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Ando in view of Komuro (U.S. Patent 6,204,543). Applicants respectfully traverse.

Independent claim 1 recites, in part:

> wherein, in said first diamond semiconductor, a conductor exhibits **an electron concentration negatively correlated with temperature in a temperature range which has a width of 100°C or more and is included within a temperature region from 0°C to 300°C**.

As an illustrative and non-limiting example of claim 1, FIG. 3 of the present application discloses a temperature region of from 0°C to 300°C, in which carrier concentration (an electron concentration in the case of first diamond semiconductor because it has n type conduction) is negatively correlated with temperature. Also, as shown in FIG. 4 of this application, a temperature region of from 0°C to 300°C is exhibited in which the Hall coefficient is positively correlated with temperature.

As is well known, anticipation under 35 U.S.C. § 102 requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed Cir. 1987). The elements must be arranged as required by the claim. *In re Bond*, 910 F. 2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). At a minimum, the cited prior art reference does not disclose (expressly or inherently) or suggest the above recited highlighted (bolded) element.

In order to establish *prima facie* obviousness under 35 U.S.C. § 103(a), all the claim limitations must be taught or suggested by the prior art. Further, "rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn*, 441 F. 3d 977, 988 (Fed. Cir. 2006). At a minimum, the cited prior art references do not disclose (expressly or inherently) or suggest the above recited highlighted (bolded) element.

The Office Action, at pages 4 an 5, asserts that all of the elements of claim 1 are allegedly disclosed by Ando at FIG. 3, and paragraphs [0018], [0020], and [0032]. However, these paragraphs merely recite:

> [0018] The n type diamond semiconductor crystal layers 4 and 7 should just be about 1 nm or more, although thickness is about 1 micrometer. The sulfur concentration doped as a donor is more than 10 $^{13}cm^{-3}$, and a maximum is a 10 $^{21}cm^{-3}$ grade.
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> [0020] Next, the characteristic of the ultraviolet ray emitting device of this invention is explained. Drawing 4 is a figure showing the analysis result of the depth direction of the impurity in the diamond semiconductor device shown by drawing 3 (b). By secondary ion mass spectrometry ("SIMS" is called hereafter.), analyze the ultraviolet ray emitting device 20 and the depth direction profile, The n type diamond semiconductor crystal layer 7 which carried out the sulfur dope from the surface of the first pass, the p type diamond semiconductor crystal layer 5 which the secondary layer **********(ed), and the insulator diamond substrate 3 of the range shown by a figure Nakaya seal are shown in drawing 4. The profile shown by a and b is a background among drawing 4.
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> [0032] In the microwave plasma CVD, atmospheric pressure is in about 30 to 60 Torr, and it was referred to as 40Torr in this embodiment. In microwave discharge, glow discharge is maintained by a comparatively high pressure. Although the temperature of the substrate which deposits makes a diamond 700 ** - 1100 **, in this embodiment, it is 830 **. Although a diamond semiconductor layer is grown homoepitaxially to the field (100) of an insulator diamond substrate, not only a field (100) but a field and a field (110) may be sufficient, for example (111). [Note, the asterisks occur in the English language machine translation of Ando.]

Therefore, Applicants submit that Ando does not teach or suggest "a conductor exhibits an electron concentration negatively correlated with temperature in **a temperature range which has a width of 100°C or more** and is included within **a temperature region from 0°C to 300°C**," as recited by claim 1.

The Office Action, at page 5, asserts that "the properties of the applicant's invention" are inherent in the device of Ando. However, "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows form the teachings of the applied prior art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). See MPEP 2112(IV). **Therefore, the assertions of inherency in the Office Action lack adequate basis in fact and/or technical reasoning, and are traversed by the Applicants.**

In Ando, the n type diamond semiconductor (as described in paragraph [0024]) is produced by a method disclosed in JP11-124682A. WO00/58534 is an English language reference which claims priority to JP11-124682A, and which describes (in detail and in English) the method and product of Ando.

In contrast with claim 1, the n type diamond semiconductor of Ando (as shown in Fig. 6 of WO00/58534) exhibits only a carrier concentration (namely electron concentration) positively correlated with temperature, and the S element has an activation energy of 0.38eV and a single donor level. Further, as shown Figs. 11, 12, 13 of WO00/58534, the n type diamond semiconductor of Ando et al. has an extremely high crystalline.

Also, in contrast with claim 1, the n type diamond semiconductor of Hasegawa et al. (US2002/0127405) is produced by the method described in paragraph [0037] of Hasegawa et al. The n type diamond semiconductor, as shown in Fig. 6 of Hasewagawa, exhibits carrier concentration positively correlated with temperature (the relationship between the vertical axis and the upper lateral axis), wherein the kind of carrier is considered on the basis of the result of Hall coefficient measurement, as described in paragraph [0035] of Hasegawa et al. Thus, an n type diamond semiconductor cannot be realized by using prior art as described in paragraph [0029] of Hasegawa et al.

Additionally, in contrast with claim 1, the n type diamond semiconductor of Yoshida et al. (USP No. 6,340,393) has a low resistance n type diamond thin film (as described in column 2, after line 15 of Yoshida et al.) and is not activated due to a deep donor level of 50 meV. Further, Yoshida et al. realized the n type diamond semiconductor by doping p type dopant and n type dopant at the same time. By the simultaneously doping n type and p type dopants, the obtained n type diamond semiconductor becomes a single crystalline diamond thin film with a low

resistance and high quality in which the n type dopant becomes stable by a high concentration, an impurity level is shallow, and the number of carrier becomes very large. In other words, it is clear that the n type diamond semiconductor of Yoshida et al. exhibits only electron concentration positively correlated with temperature such that the number of carrier increases along with the shallowing of an impurity level.

Accordingly, the n type diamond semiconductor according to **claim 1 requires electron concentration negatively correlated with temperature,** whereas the n type diamond semiconductors of the three cited references exhibit electron concentration positively correlated with temperature.

Thus, Applicants submit that claim 1 is not anticipated by Ando, and is not obvious in view of Ando. Further, the other cited prior art references (Hasegawa, Yoshida and Komuro) do not remedy the deficiencies of Ando.

Hasegawa, at paragraphs [0037] to [0038], merely discloses n type diamond semiconductor fabricated by ion implantation, and does not teach or suggest, "**an electron concentration negatively correlated with temperature in a temperature range which has a width of 100°C or more and is included within a temperature region from 0°C to 300°C**," as recited by claim 1.

Yoshida, at column 2, lines 51-52, merely discloses simultaneously doping a p type dopant and an n type dopant, and does not teach or suggest, "**an electron concentration negatively correlated with temperature in a temperature range which has a width of 100°C or more and is included within a temperature region from 0°C to 300°C**," as recited by claim 1.

Komuro, at column 3, lines 57-63, merely discloses ion-implantation forming a low density impurity diffusion layer in the drain formation planned region, and does not teach or suggest, "**an electron concentration negatively correlated with temperature in a temperature range which has a width of 100°C or more and is included within a temperature region from 0°C to 300°C**," as recited by claim 1.

Thus, at a minimum, the combination of Ando and Hasegawa and Yoshida and Komuro. fails to teach or suggest the forgoing element, and therefore claim 1 is allowable over the cited art.

Similar to claim 1, independent claim 15 recites, in part, "a conductor exhibits **an electron concentration negatively correlated with temperature in a temperature range which has a width of 100°C or more and which is included within the temperature region from 0°C to 300°C**."

Thus, Applicants submit that independent claim 15 is allowable for at least the same reasons as claim 1.

Under Federal Circuit guidelines, a dependent claim is allowable if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987).

Thus, as independent claims 1 and 15 are allowable for the reasons set forth above, it is respectfully submitted that dependent claims 2-14 and 16 are allowable for at least the same reasons as their respective base claims.

Accordingly, it is urged that the application, as now amended, is in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues

that might be resolved by an interview or an Examiner's amendment, Examiner is requested to call the undersigned attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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